

FIG. 1

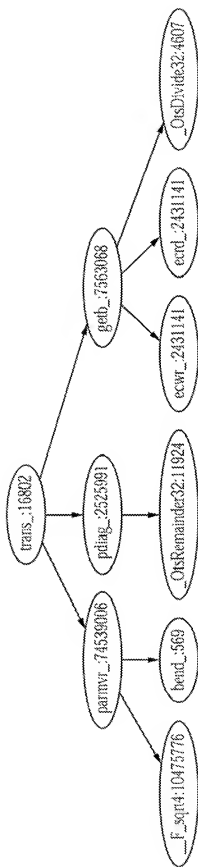


FIG. 2

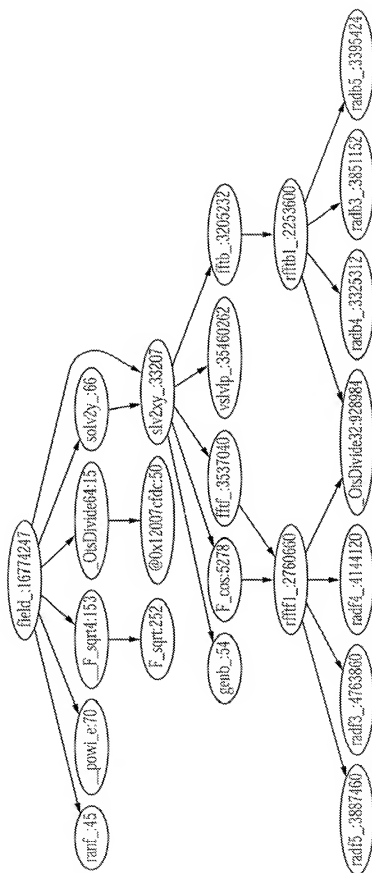


FIG. 3

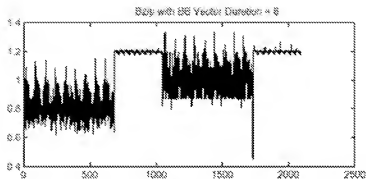


FIG. 7A

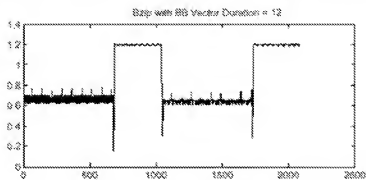


FIG. 7B

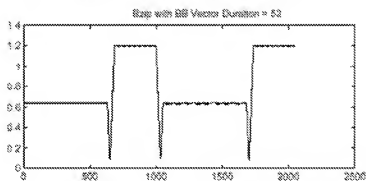


FIG. 7C

Instruction Cache	32k 2-way set-associative, 32 byte blocks, 1 cycle latency
Data Cache	64k 4-way set-associative, 32 byte blocks, 2 cycle latency
Unified L2 Cache	1 Meg 4-way set-associative, 32 byte blocks, 12 cycle latency
Branch Predictor	hybrid - 8-bit gshare w/ 8k 2-bit predictors + a 8k bimodal predictor
Out-of-Order Issue	out-of-order issue of up to 8 operations per cycle, 128 entry re-order buffer
Mechanism	load/store queue, loads may execute when all prior store addresses are known
Architecture Registers	32 integer, 32 floating point
Functional Units	8-integer ALU, 4-load/store units, 2-FP adders, 2-integer MULT/DIV, 2-FP MULT/DIV
Virtual Memory	8K byte pages, 30 cycle fixed TLB miss latency after earlier-issued instructions complete

FIG. 8

name	init	period	bpred	ruu	IPC	d miss	i miss	val miss	addr miss
bzip	2	9	4.2%	75.8%	2.681	1.7%	0.000%	25.1%	13.3%
hydro	5	17	0.4%	68.7%	0.793	14.6%	0.022%	8.3%	0.6%
tomcat	13	5	0.8%	59.6%	0.955	9.7%	0.043%	46.2%	1.0%
vortex	40	144	0.6%	43.4%	2.726	0.9%	0.979%	15.2%	16.4%
vpr	4	2	9.3%	49.8%	1.143	3.0%	0.001%	16.6%	14.2%
wave	68	70	0.6%	62.2%	2.596	7.4%	0.000%	38.1%	7.9%

FIG. 10

name	start	bpred	err	ruu	err	IPC	err	data	err	inst	err	val	err	addi	err
bzip	150	4.2%	1%	75.4%	0.5%	2.8	5.1%	1.3%	25.8%	0.0%	-	25.4%	1.1%	15.7%	17.9%
hydro	6	0.3%	16%	69.8%	1.7%	0.8	2.5%	14.8%	1.5%	0.0%	-	8.2%	1.8%	0.6%	9.1%
tomcat	12	0.8%	3%	60.5%	1.5%	0.9	1.5%	9.8%	1.1%	0.0%	-	41.1%	12.4%	0.9%	17.1%
vortex	382	0.6%	2%	43.7%	0.8%	2.8	1.9%	0.9%	1.2%	1.0%	2.8%	15.2%	0.1%	16.3%	0.7%
vpr	746	9.0%	3%	49.7%	0.3%	1.2	4.3%	3.1%	6.4%	0.0%	-	16.6%	0.0%	14.4%	1.3%
wave	127	0.6%	9%	60.7%	2.5%	2.5	3.3%	7.7%	4.4%	0.0%	-	40.4%	6.1%	8.5%	7.8%

FIG. 11

name	start	bpred	err	ruu	err	IPC	err	data	err	inst	err	val	err	addi	err
bzip	1733	4.0%	6%	63.8%	18.8%	2.5	5.9%	1.8%	8.0%	0.0%	-	14.2%	77.2%	7.3%	82.0%
hydro	36	0.3%	12%	69.2%	0.9%	0.8	3.9%	14.8%	1.4%	0.0%	-	8.4%	0.4%	0.6%	9.3%
tomcat	144	0.8%	1%	60.9%	2.2%	1.0	1.9%	9.5%	2.0%	0.1%	-	39.8%	16.2%	1.1%	13.7%
vortex	330	0.6%	3%	41.9%	3.5%	2.8	3.4%	0.7%	16.3%	1.0%	4.0%	15.7%	3.8%	17.7%	7.7%
vpr	746	9.0%	3%	49.7%	0.3%	1.2	4.3%	3.1%	6.4%	0.0%	-	16.6%	0.0%	14.4%	1.3%
wave	1036	0.3%	84%	61.5%	1.2%	2.8	6.0%	7.9%	6.7%	0.0%	-	37.0%	2.8%	6.5%	20.8%

FIG. 12

name	start	bpred	err	ruu	err	IPC	err	data	err	inst	err	val	err	addi	err
bzip	11	4.9%	17%	74.3%	2.0%	2.2	23.2%	2.8%	68.9%	0.0%	-	22.7%	10.8%	8.5%	55.4%
hydro	22	0.3%	12%	69.6%	1.4%	0.8	2.4%	14.8%	1.7%	0.0%	-	8.5%	1.8%	0.6%	8.6%
tomcat	18	0.6%	28%	61.0%	2.4%	0.9	4.6%	10.1%	5.1%	0.0%	-	44.0%	6.1%	0.3%	23.7%
vortex	184	0.4%	42%	46.4%	6.9%	3.2	17.6%	0.9%	6.1%	0.7%	36%	14.8%	2.3%	16.2%	1.6%
vpr	6	1.1%	740%	58.1%	16.6%	3.0	162%	0.4%	62.1%	0.0%	-	16.6%	0.2%	13.8%	2.6%
wave	138	0.9%	55%	60.5%	2.8%	2.4	9.1%	7.3%	1.1%	0.0%	-	40.1%	5.5%	7.7%	2.3%

FIG. 13

Instruction Cache	8k 2-way set-associative, 32 byte blocks, 1 cycle latency
Data Cache	16k 4-way set-associative, 32 byte blocks, 2 cycle latency
Unified L2 Cache	1 Meg 4-way set-associative, 32 byte blocks, 20 cycle latency
Memory	150 cycle round trip access
Branch Predictor	hybrid - 8-bit gshare w/ 8k 2-bit predictors + a 8k bimodal predictor
Out-of-Order Issue	out-of-order issue of up to 8 operations per cycle, 128 entry re-order buffer
Mechanism	load/store queue, loads may execute when all prior store addresses are known
Architecture Registers	32 integer, 32 floating point
Functional Units	8-integer ALU, 4-load/store units, 2-FP adders, 2-integer MULT/DIV, 2-FP MULT/DIV
Virtual Memory	8K byte pages, 30 cycle fixed TLB miss latency after earlier-issued instructions complete

FIG. 14

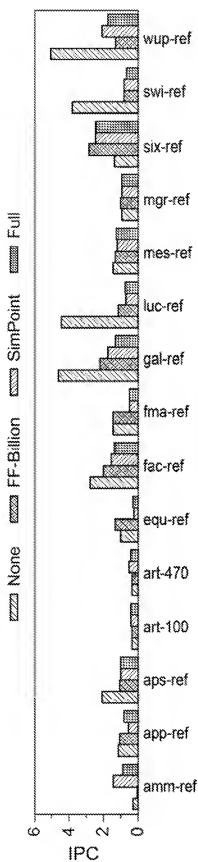


FIG. 23A

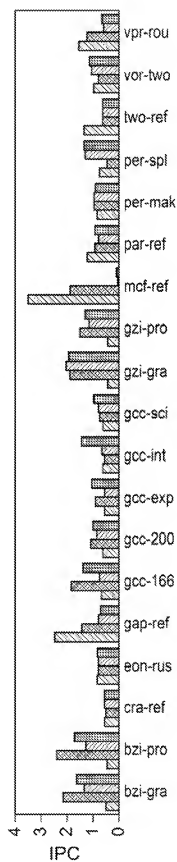


FIG. 23B

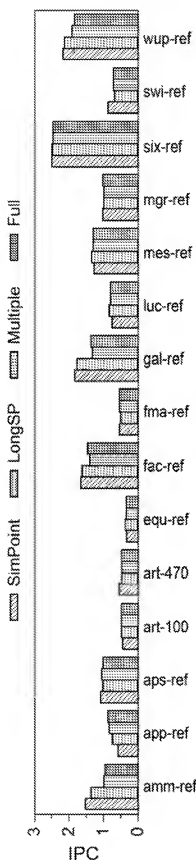


FIG. 25A

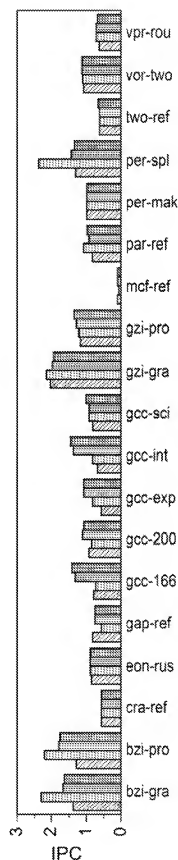


FIG. 25B

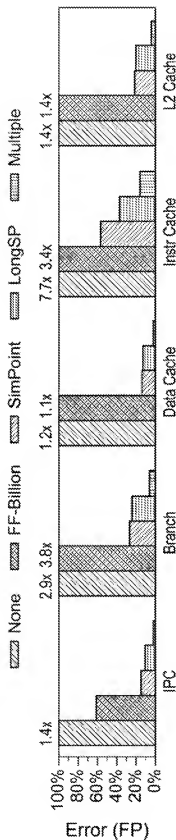


FIG. 26A

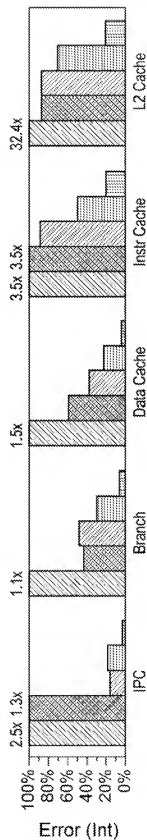


FIG. 26B

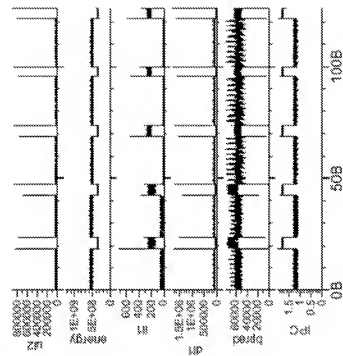


FIG. 27B

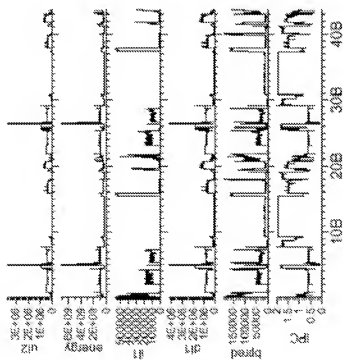


FIG. 27A

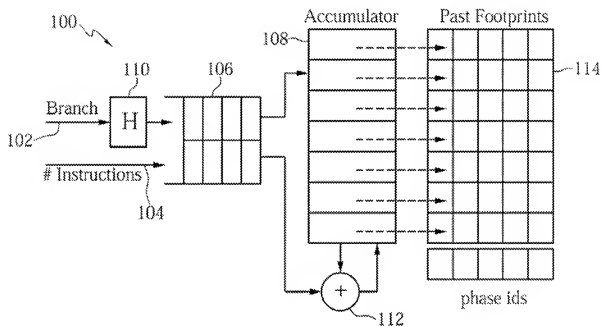


FIG. 28

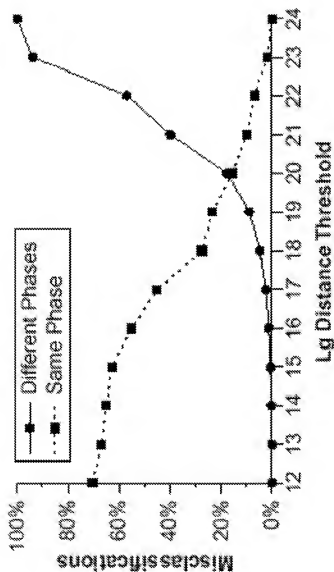


FIG. 32

phase	IPC (stddev)	bpred (stddev)	dl1 (stddev)	il1 (stddev)	energy (stddev)	ul2 (stddev)
full	1.32 (43.4%)	27741 (135.5%)	445083 (110.7%)	50763 (203.2%)	6.44E+08 (90.0%)	227912 (139.7%)
18.5%	0.61 (1.6%)	34665 (22.0%)	753382 (5.4%)	125091 (23.2%)	1.03E+09 (1.8%)	395997 (5.3%)
18.1%	1.95 (0.3%)	13048 (3.9%)	28112 (15.1%)	43 (73.9%)	3.22E+08 (0.2%)	1006 (5.6%)
7.2%	0.64 (0.2%)	843 (15.1%)	885081 (0.1%)	75 (215.5%)	9.78E+08 (0.3%)	443655 (0.1%)
4.0%	1.49 (1.2%)	10145 (7.6%)	703554 (6.8%)	15591 (5.2%)	4.20E+08 (1.1%)	354084 (7.0%)
3.9%	1.76 (1.6%)	2015 (13.6%)	98947 (5.9%)	102 (45.1%)	3.57E+08 (1.6%)	15595 (12.6%)
phase	IPC (stddev)	bpred (stddev)	dl1 (stddev)	il1 (stddev)	energy (stddev)	ul2 (stddev)
full	1.33 (16.3%)	56045 (11.1%)	90446 (58.2%)	60 (138.1%)	4.82E+08 (13.5%)	22880 (112.0%)
17.1%	1.24 (3.4%)	53300 (10.8%)	96960 (10.1%)	12 (44.2%)	5.05E+08 (3.5%)	24218 (8.6%)
9.4%	1.23 (3.8%)	54973 (11.5%)	99523 (11.3%)	11 (45.5%)	5.09E+08 (3.8%)	24518 (9.3%)
8.8%	1.76 (0.6%)	56449 (4.8%)	37331 (5.6%)	241 (8.4%)	3.55E+08 (0.6%)	5617 (15.6%)
8.0%	1.22 (4.3%)	54791 (6.8%)	99671 (11.9%)	40 (25.7%)	5.14E+08 (4.4%)	28153 (11.0%)
7.4%	1.24 (3.1%)	55215 (11.1%)	96701 (9.6%)	12 (35.4%)	5.04E+08 (3.2%)	23701 (8.4%)

FIG. 33

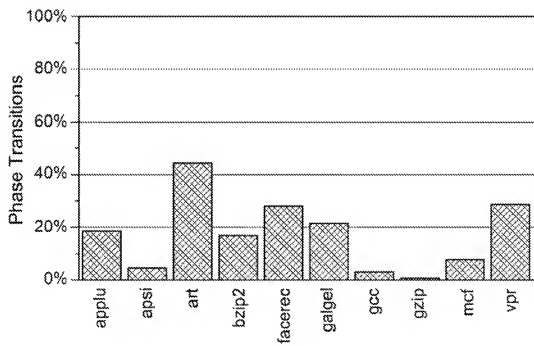


FIG. 34

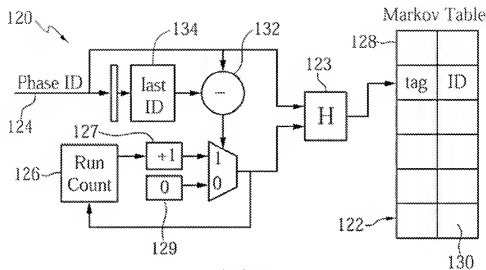


FIG. 35

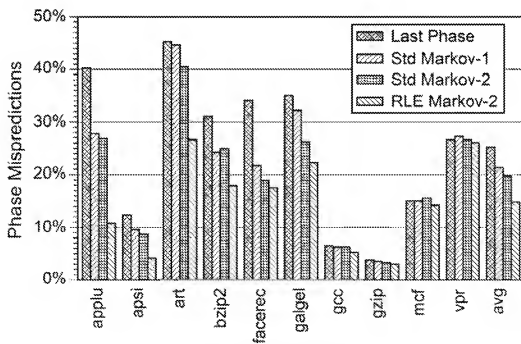


FIG. 36